MULTIPLEXER

A Thesis Submitted

In Partial Fulfilment of the Requirements

for the Degree of

MASTER OF TECHNOLOGY

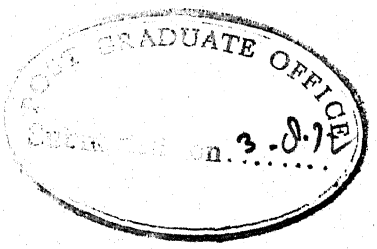
BY

RAJ KUMAR MANOCHA

TO THE

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY



CERTIFICATE

Certified that this work on "MULTIPLEXER" by Mr. Raj Kumar Manocha has been carrie d out under my supervision and that this has not been submitted elsewhere for a degree.

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This thesis has been approved for the award of the Degree of Master of Technology (M.Tech.) in accordance with the regulations of the Indian Institute of Technology Kanpur
Dated. 6/9/72

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SYNOPSIS

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Multiplexer

Design and fabrication of solid state "Multiplexer" using FET's is described. It consists of two sections, first section takes in the digital selection input from IBM 1800 computer, checks for device code, decodes the incoming selection input and generates a reset pulse. The second section receives analog inp from the transducer and connects them to the output terminal through analog switches. These switches are turned ON or OFF by selection input.

The multiplexer can have upto 1024 analog inputs, but in the present set up only 16 analog input points have been provided.

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LIST OF FIGURES

INTRODUCTION

The word multiplexer comes from the Latin words 'MULTI' + 'PLEX' which means multifold.

For automatic control of a number of processes with one computer it is desirable that the interface between the process and the computer is not duplicated for all the processes. This necessitates the use of a system which requires only one interface, but connects all the processes to the interface as per requirements. The system which connects the fifferent processes with the interface under the control of computer is called the multiplexer.

Thus the multiplexer is a system which selects a channel out of a group of channels for a fixed amount of time. Examples of multiplexer switches are band switches, rotatory switches, relay switches and solid state device switches. In rotatory switches the channels are selected sequentially and random mode of selection is not possible. For random selection of channels relay and solid state multiplexers are used. In relay multiplexers speed is limited by mechanical movements of the relays. To attain high multiplexing rates solid state multiplexer is used. Moreover the size, cost and power consumption is much less for a solid state multiplexer as compared to relay multiplexer of same number of channels.

Basically a multiplexer is a group of switches and any one of them can be closed as per requirement. Each of the individul switch should have very high resistance when open and as low resistance as possible when it is closed. In this multiplexer field effect transistors have been used successfully against the bipolar transistors as analogswitches.

The multiplexer receives the channel address from digital output terminals of IBM 1800 computer. The channel address which is in binary form is decoded by using digital integrated circuits.

The multiplexer can accept selection input which consists of device address and channel address from any system which satisfies the input voltage level conditions.

SYSTEM DESIGN CONSIDERATIONS

In this chapter we discuss the various parts of this multiplexer unit and different possible schemes to achieve the various functions.

1.) Input to the multiplexer

The address of the channel to be multiplexed is obtained from digital output terminals of IBM 1800 computer. This output can be in three forms:

(A) ECO (Electronic Contact Operate)

(B) Pulse Form

(C) Register Form

In ECO 16 relay contacts are closed or open according to the bit pattern.

In pulse form a pulse appears whenever 'one' has to appear in output, and no pulse wherever 'zero' has to appear. Simultaneously 16 pulses can appear which form one word.

In register form one 16 bit word of IBM 1800 is loaded into the register

In all these forms channel address obtained from digital output terminals of IBM 1800 computer is coded in binary.

2.) Device Code

If in the digital output six highest order bits have 100000 combination, then the rest 10 bits are taken in as multiplexer channel address. This is just to check that the digital output is addressing the multiplexer and no other device. When the 6 high order bits have the multiplexer code, the output of a gate changes from "0" level to "1" level and it remains in that state till the multiplexing of required channel is in progress.

3.) Check for Multiplexer Busy

If in the digital output we get a valid multiplexer address

and the multiplexing of some channel is in progress, then we will be multiplexing a channel whose address is the "OR" of the addresses of channel in progress and new channel. The input to the ADC will be (i) the voltage of channel in progress for small fraction of total multiplexing time (ii) the voltage of the channel which has the ORed address of previous and new channels, for the rest of the multiplexing time. To avoid this we check for the presence of match pulse. If the match pulse is there which means the multiplexing of the channel is in progress, then any incoming input is debarred from reaching the storage elements in the multiplexer.

4.) Generation of Reset Pulse

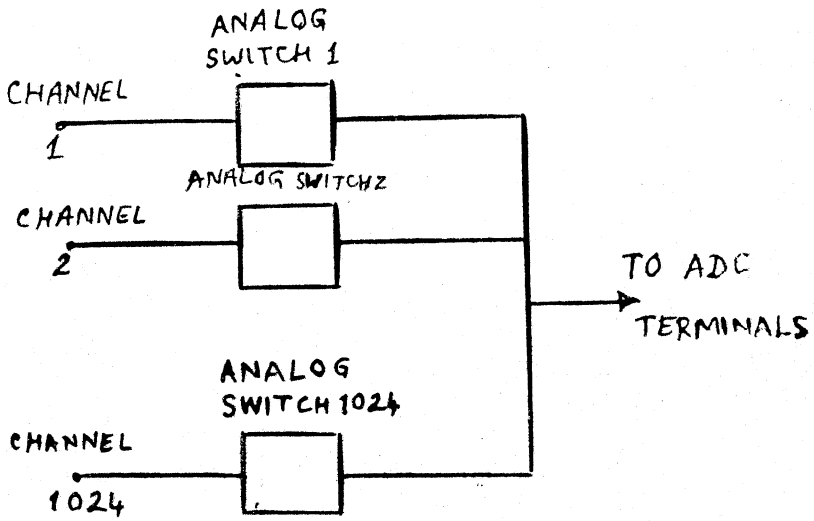
Whenever a digital output which does not represent a valid multiplexer channel address or whenever the multiplexing of a channel is over, the multiplexer should be reset and made ready for the next input.

Thus (i) if we do not get the code for multiplexer and some output appears in digital output terminals of IBM 1800 computer, that is at least one bit is in "1" state, then a reset pulse is generated which clears the buffer.

(ii) if a valid multiplexer channel address is obtained then the resetting is delayed by an amount equal to multiplexing time for one channel. The delay is introduced by using a one shot multivibrator.

5.) Decoding of Address

(A) In the simplest decoding form of taking 1024 lines from 10 bit binary address we have to put a series switch with each channel (see figure 2.1) and the other end of all the switches are connected to the input terminals of ADC. For 1024 channels the output capacitance of switch will be multiplied which will appear as a very high



ONE LEVEL DECODING SCHEME FOR 1024 CHANNEL MULTIPLEXE

FIG 2·1

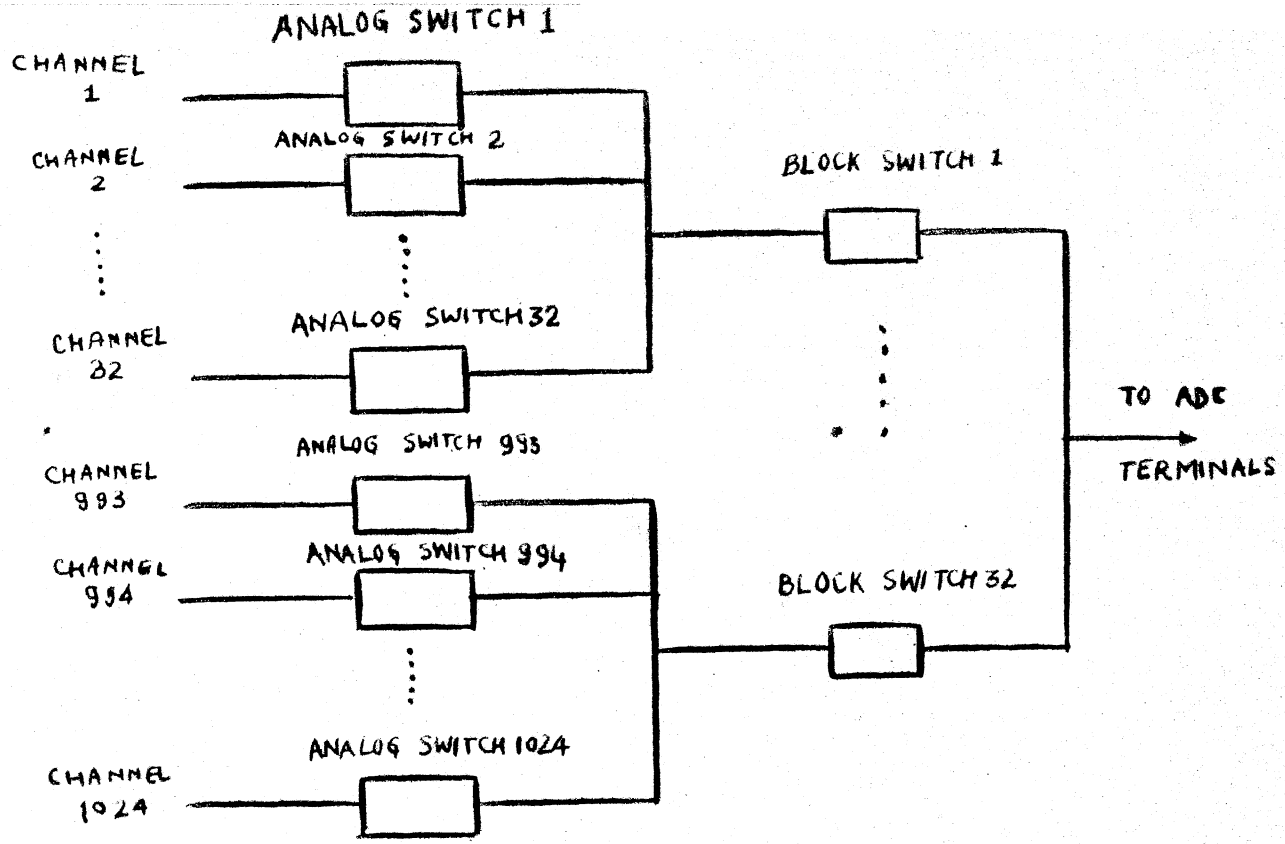
capacitance at the input terminals of ADC thus unnecessarily increasing the rise time. This necessitates to modify this scheme of decoding.

(B) In another scheme decoding is done in number of levels. In two level decoding a group of 32 chennels is connected to a switch called the block switch, and there are 32 block switches thus giving rise to 1024 channels. In this way the effective output capacitance at ADC terminals is of 32 switches only. As for as decoding is concerned, ten bits are divided in two groups. First group of 5 bits selects a block switch and second group of 5 bits selects the channel in each of 32 block switches. So we require 2 decoders, each one of them is 1 out of 32, and we put 32 additional switches at the cost of reduced capacitance at ADC terminals.

In three level decoding there are four group switches, each group switch has 16 block switches and each block switch has got 16 individual switches. Thus at the input terminals of ADC output capacitance of only 4 switches appears and also at the input of block switches output capacitance of only 16 switches is there. But here we use 68 additional switches for reducing the rise time at ADC terminals.

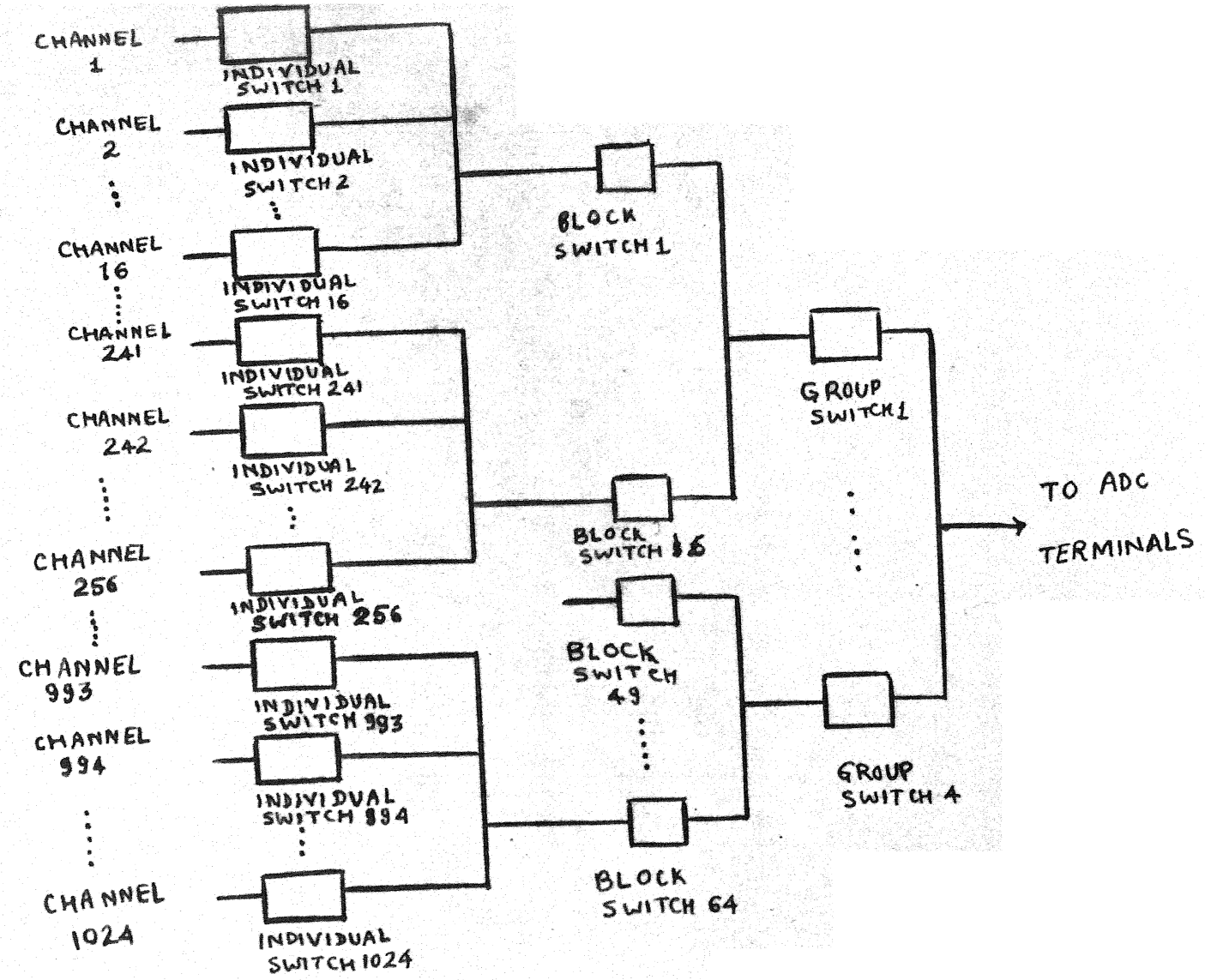
In four level decoding the number of additional switches is quite large and is 146. Also the fanout of individual switch driver is 128 which is a very high value.

(C) Still another scheme for decoding is to have a unit containing analog switches and its associated decoder. Commercially a multiplexer unit is available which consists of 1 out of 8 decoder and 8 analog switches. Let us say we have to make 64 channel multiplexer using such multiplexer units. We have to put in two levels of decoding units (see figure 2.4). Here 1 out of a 8 decoder is duplicated number of times. If the decoder has to be made using discrete components then this scheme becomes very expensive.



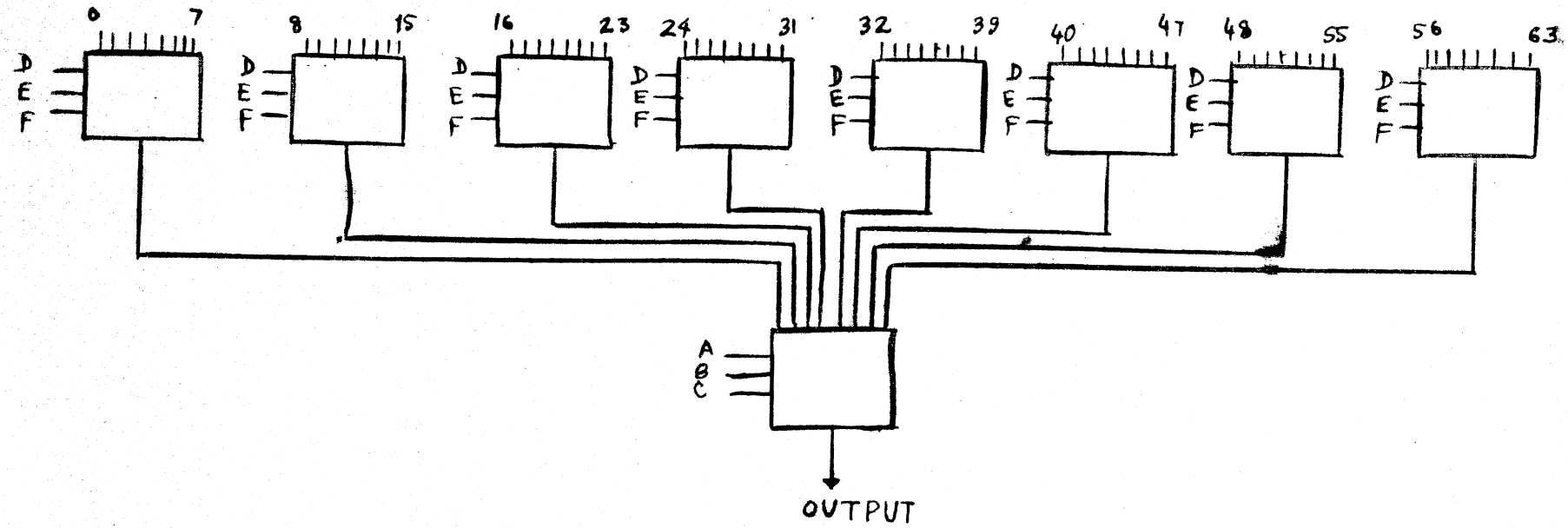
BLOCK DIAGRAM FOR
2 LEVEL DECODING
OF 1024 CHANNELS

FIG 2-2



BLOCK DIAGRAM FOR 3 LEVEL DECODING OF 1024 CHANNELS

FIG 2.3



64 CHANNEL MULTIPLEXER USING BUILT-IN MULTIPLEXER UNITS

FIG 2.4

6.) Buffer

Since (i) in case of pulse form of selection input, pulse width is programmable, and (ii) the selection input can arrive at a rate faster than the sampling rate of the multiplexer, so it becomes essential to put the chennel address in a buffer till the process of multiplexing of that channel is over.

One way to store the information is to store in a flip-flop. In TT L family of digital integrated circuits, standerd chips of JK flip-flops are available. These flip-flops have the additional facility of clearing all the stored information by giving input to an overiding input terminal. Even RS flip-flop can be used but these are not commerially available in TT L family.

7.) Analog Switch

The various types of analog switches are

(A) Semiconductor diode analog switch

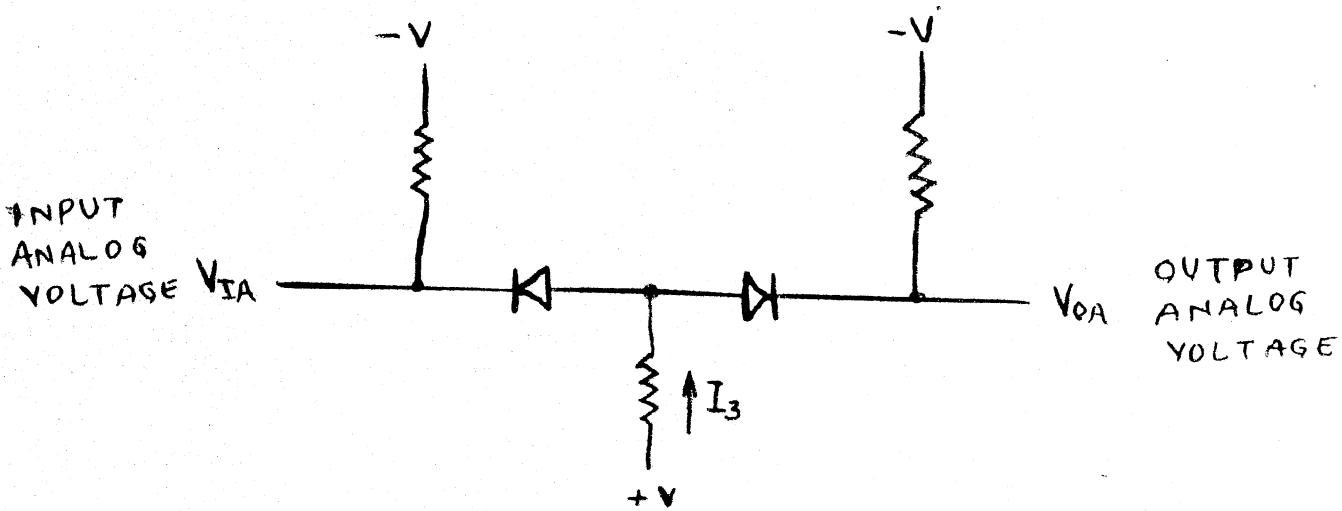
(B) Bipolar Transistor Analog Switch

(C) Junction Field Effect Transistor

(D) MOS Field Effect Transistor

(A) In semiconductor diode analog switch the offset voltage (the voltage across the output terminals of a switch with no current flowing between these terminals) is very high. Though by using matched diodes (see figure 2.5) some of the offset voltage errors can be removed but the capacitance across back biased junction limits the speed of switching to a great extent.

(B) In bipolar transistor switch offset voltage is dependent on base current and temperature. At lower values of base current the offset voltage is fairly high and decreases with the increase of base current and at high base currents offset voltage increases as the bulk resistances become predominate. At higher values of base currents increase of h_{FE} with temperature tends to decrease the offset voltage and the collector bulk



ANALOG SWITCH USING SEMICONDUCTOR DIODES (BACK TO BACK)

FIG 2.5

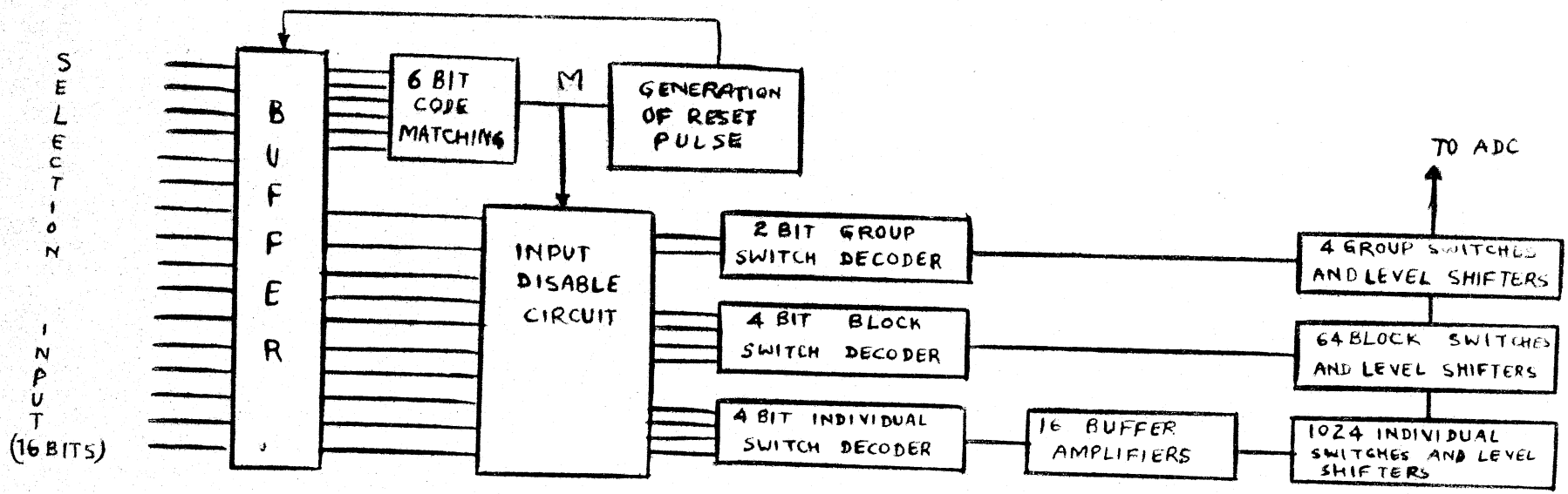
resistance is tending to increase offset voltage as temperature increases. With the increase of base current saturation resistance of the transistor decreases until the emitter and collector bulk resistances put a limit on saturation resistance. At low base currents saturation resistance is linear function of temperature and since collector and emitter bulk resistances have positive temperature coefficients, the saturation resistance will usually have a positive temperature coefficient.

By using matched transistor offset voltage can be reduced, but at the cost of saturation resistance.

(C) In junction field effect transistor for a gate-to-source voltage of zero volt, no offset voltage even of the order of a few microvolts will be there. When gate-to-source voltage is not zero, the offset is due to leakage currents flowing across the back biased gate-to-source and gate-to-drain junctions, and its magnitude depends upon the resistance of the circuitry connected to the drain and source. By keeping the gate-to-source voltage zero the saturation resistance of the device is minimised. Also there is no problem with drive currents flowing into the analog voltage source as JFET is a voltage controlled device.

(D) In MOS field effect transistor there are absolutely no problems of drive currents flowing in to the analog voltage source but this device suffers very badly from the lower limit of input frequency which is usually of the order of 10 Kc/s.

Thus for the analog switch to be used in this multiplexer MOSFET and semiconductor diode analog switches are out. The choice is left between bipolar transistor and JFET. The only advantage which the bipolar transistor has over JFET is lower saturation resistance. By putting an operation amplifier at output terminals the above said drawback in JFET is nullified because the input impedance ism of the



BLOCK . DIAGRAM

OF

MULTIPLEXER

FIG 2.6

CHEPTER III

HARDWARE DESIGN

(1) Design of Analog Switch

(i) The junction field effect transistor to be used in the circuit should be fast switching transistor.

(ii) Saturation resistance of the JFET should be very small.

(iii) The leakage currents which are due to reverse biased gate-to-source and gate-to-drain junctions shoud should bem minimum.

(iv) Resistance between drain and source terminals should be very high when the FET is biased beyend pinch off.

(v) Reverse transfer capacitance, source to gate and drain to gate capacitances should be minimum as they distort the output waveform to a great extent.

2N5458 has the following specifications:

(i) Gate reverse current for V_{GS} = 15V_{dc}, V_{DS} = 0 is 1 nAdc.

(ii) Gate source cut off voltage for V_{DS} = 15V_{dc} l I_D = 10 nA dc is 7 V_{dc} (max.)

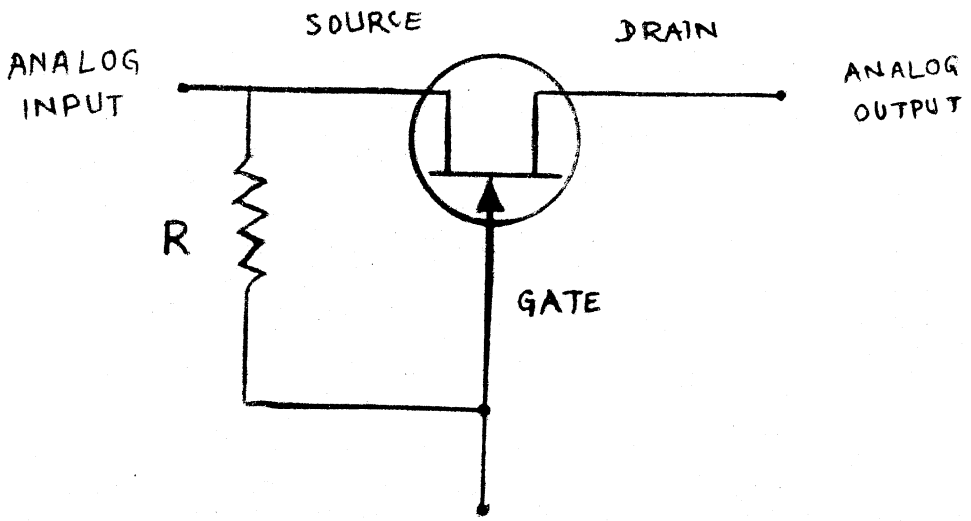
(iii) Gate source breakdown voltage for I_G = 10 A dc, V_{DS} = 0 is 25 V_{dc} (min.)

(iv) Zero gate voltage drain current for V_{DS} 15V_{dc}, V_{GS} = 0 is 9 madc.

So we find that 2N5458 meets most of the above requirements. The choice is limited because of nonavailability of other JFETS. 2N5639 is certainly a better FET than 2N5458 for this application, as per experimental results.

When the gate is kept at a high negative voltage with respect to source, (refer to figure 3.1) the FET is pinched off. From characteristics of 2N5458 gate to source cut off voltage is -7V.

Q3



FET SWITCH (WITHOUT DRIVING CIRCUITRY)

FIG 3.1

So at the gate terminal voltage level should be -12V as the input can go upto -5V.

Resistance R in the circuit plays two roles. When FET is OFF it determines the input impedance of the switch. Also it limits the current flowing out of analog source.

When FET is ON it brings the gate to the same potential as that of source, thus keeping $V_{GS} = 0$ which ensures low value of saturation resistance.

To keep the input impedance high, R should be high but input capacitance puts a limit to this, because with the increase of R rise time increases. So a value of 82 K was chosen for R which with input capacitance of 7 pf brings the rise time to 0.6 sec.

(2) Design of Level Shifter

When the input to the level shifter is "1" level (2.4V to 5V) the FET gate should go down to -12V but when the input is zero level (0V to 0.6V) the FET gate should be left unaffected. A circuit which does this job is shown in figure 3.2

Resistance R_1 determines the current drawn in from the TT L gate or from buffer amplifier (refer to the block diagram) and the value of the current I_{c1} should be such that

$$I_{c1}\ (\text{min.}) * R_2\ (\text{min.}) \qquad V_{BE2}\ (\text{sat.})$$

V_{in} for "1" level is 2.6 V.

$$I_1 = (2.6 - 0.6)/2K = 1\text{ma}$$

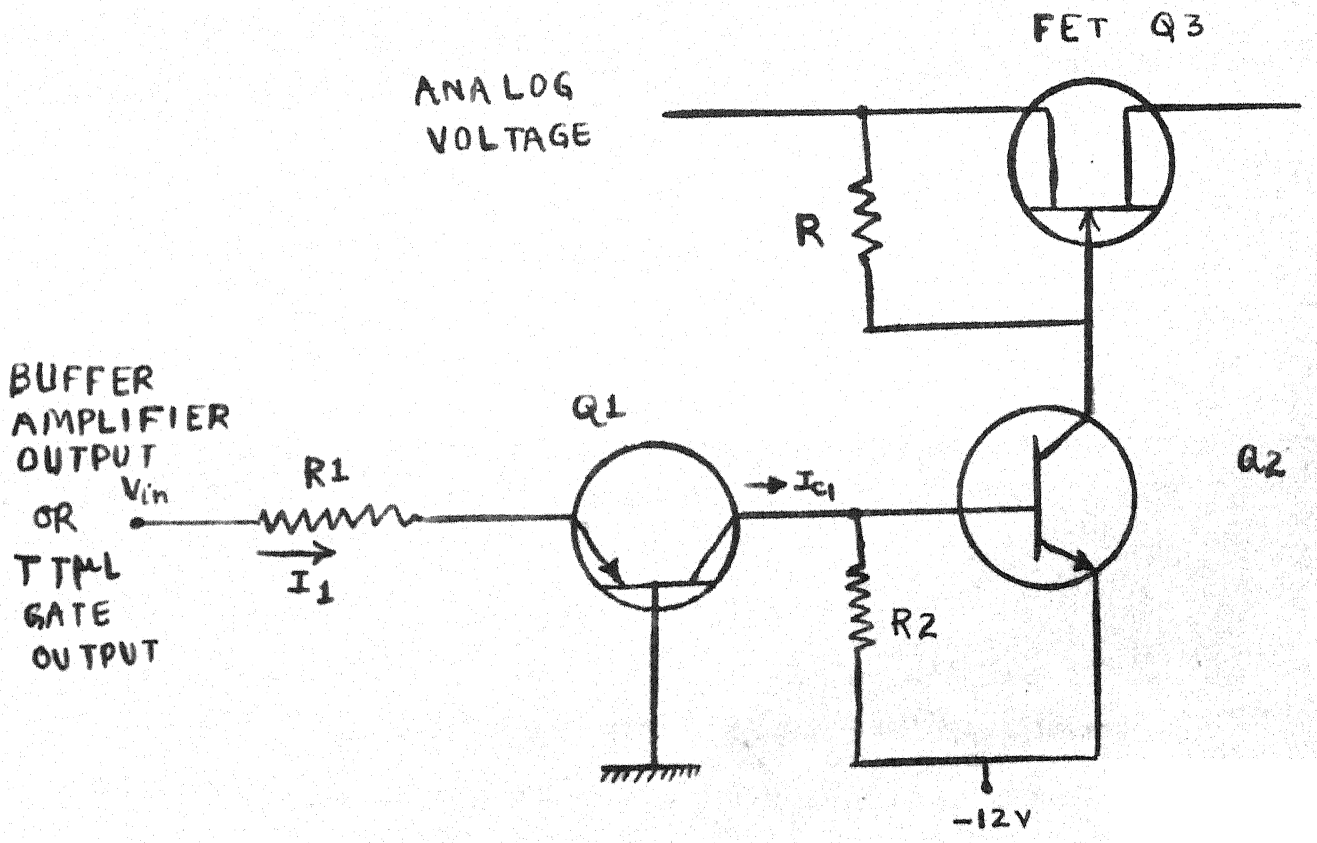
Taking = 0.9 for Q_1

$$I_{c1} = 0.9\text{ ma}$$

Now R_2 $V_{BE2}\ (\text{sat.})/I_{c1}$

0.7V/0.9 ma

0.8 K



FET SWITCH WITH LEVEL SHIFTER

FIG 3.2

Taking into account the variations in parameters, we choose R_2 as 2K which gives us additional margin.

Also Q_1 and Q_2 should be both high gain and switching transistors.

For Q_1 transistor suitable is 2N3250

For Q_2 transistor suitable is CIL 522

Both have breakdown voltages 40V which is very essential because we are putting in voltage swing of approximately 20V.

(3) Design of Decoder

Decoder takes in the address of the channel in binary form and in turn selects a switch which connects the required channel to ADC. Two decoders are there in the circuit

(A) One out of four decoder, which selects the group

(B) One out of sixteen decoder, two such decoders select block switch and individual switch respectively.

(A) One out of four decoder

The design of the decoder is straight forward and the circuit is shown in figure 3.3 when the multiplexer is in ready state to accept some input, the inputs A and B to the decoder are in "0" level which will cause them group switch zero to close which is not desirable. The group switch zero should close only when inputs A and B are zero and the 6 bit code match occurs, i.e. when Qe is 1

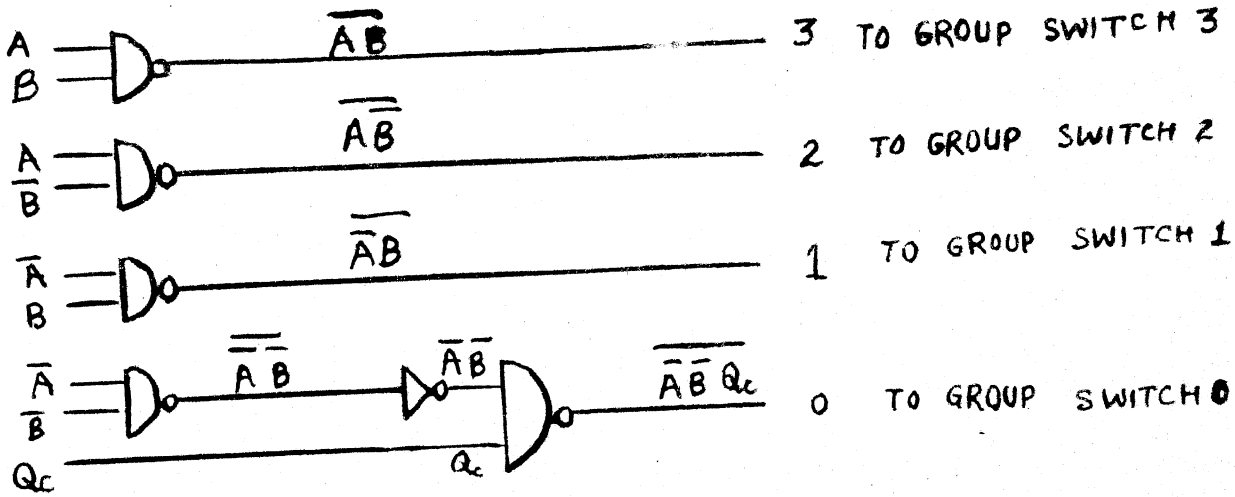
(B) Design of one out of sixteen decoder

The decoding of 4 bits A,B,C,D can be done by using

(i) 2 input gates

(ii) 3 input gates

(iii) 4 input gates



1 OUT OF 4 DECODER

FIG 3.3

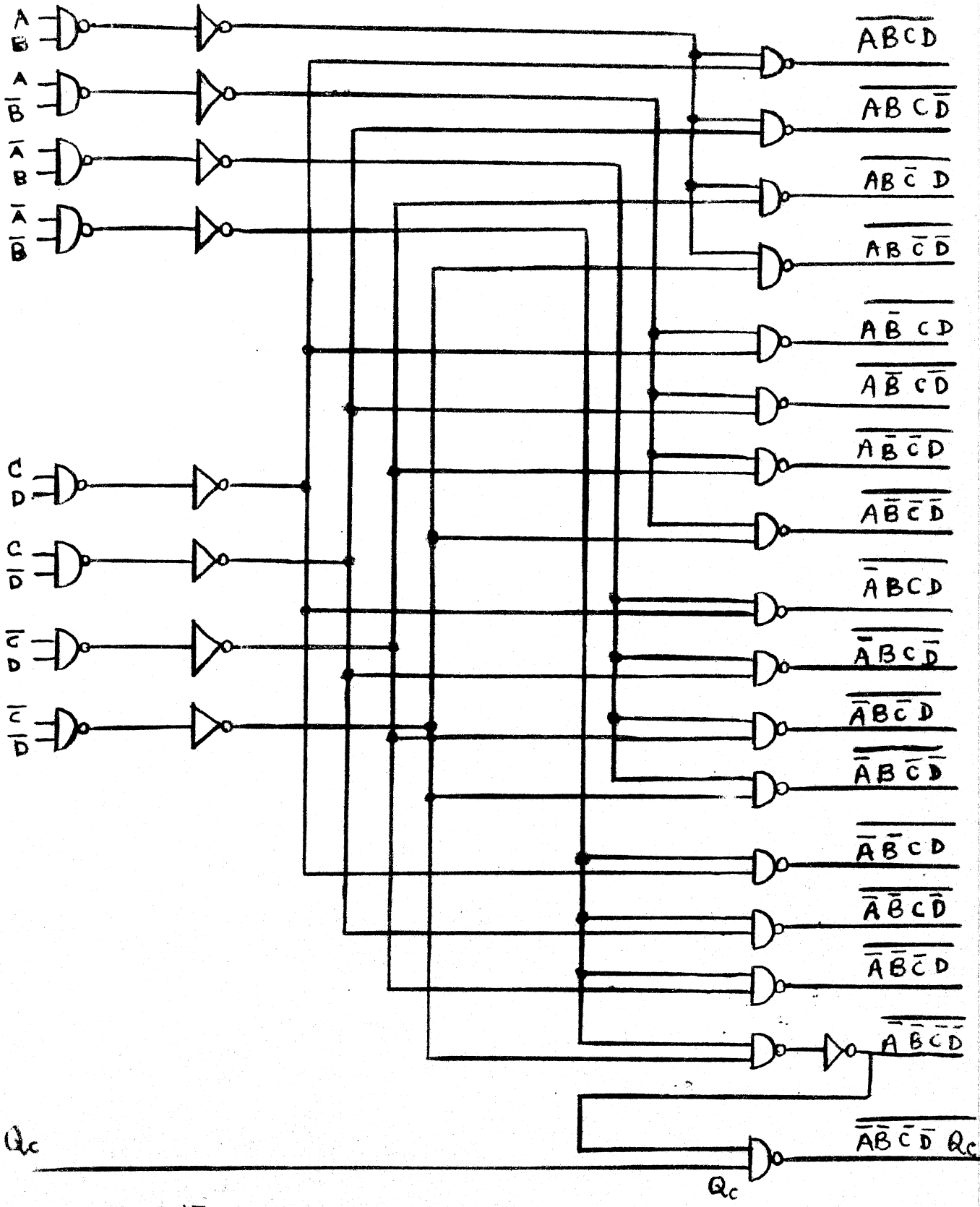
Using 2 input gates we have to use 24 two input gates and 8 invertors, which means total of 8 IC chips. (see figure 3.4).
Using 3 input gates we have to use eight 3 input gates, sixteen 2 input gates and eight invertors which brings the total number of chips to be used in the circuit to nine. (see figure 3.5)
Using 4 input gates we have to use sixteen 4 input gates which means 8 IC chips. (see figure 3.6)
The cost of each IC chips is approximately the same. So from cost point of view decoding by use of 3 input gates is ruled out. By use of 2 input gates the decoder has more number of stages than a decoder using 4 input gates, and it is not advisable to increase the decoding time. So we make use of 4 input gates for decoder.

(4) Design of Buffer Amplifiers

When all the 1024 lines are used, the fanout of 1 out of 16 decoder lines, which control the individual switches, is going to be 64. Also the current drawn out from the line by the level shifter is 1 ma. So effectivaly we require a current of 64 ma from each line of the decoder. A TT L nand gate is not capable of supplying this amount of current. So we introduce a buffer stage between TT L g output and the input of level shifter.

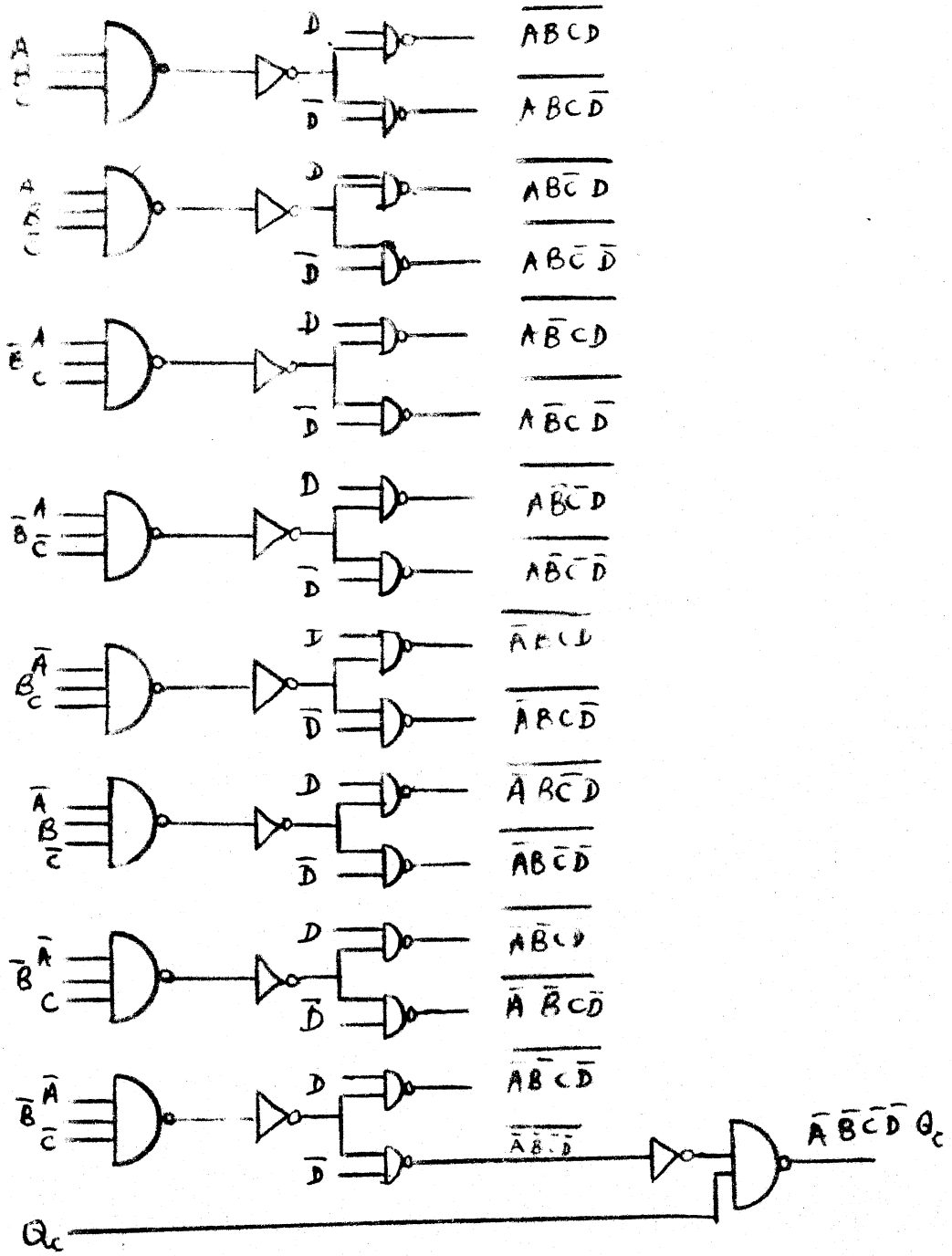
When the output voltage of a TT L gate is 4V for "1" level the current drawn by the level shifter will be approximately 2ma. So the buffer stage should be able to feed a current of approximately 128 ma.

The transistor used for buffering should have (i) the capacity to supply currents of the order of 150 ma, and also (ii) the power dissipation should be high. Since 64 lines are going to be connected at one point, so it is essential for the buffer amplifier to provide



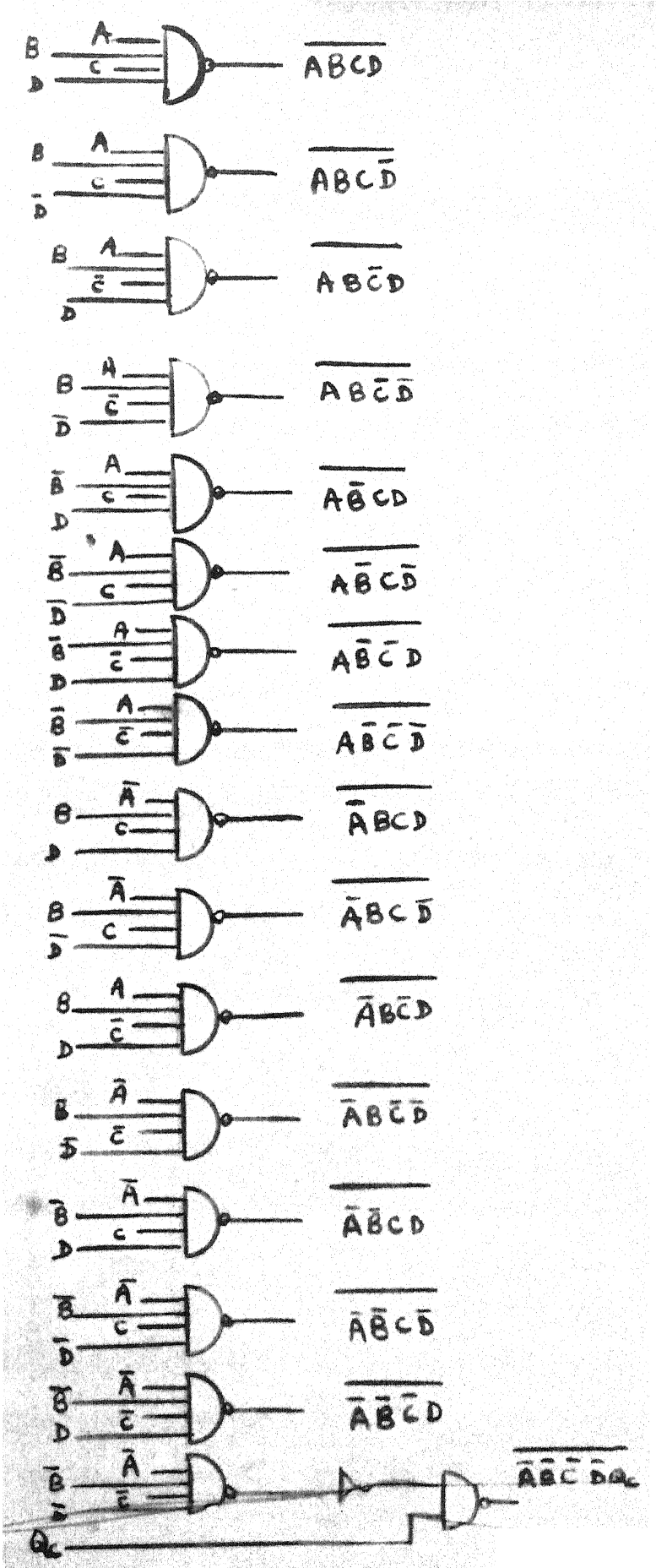
1 OUT OF 16 DECODER USING 2 INPUT GATES ONLY

FIG 3·4



1 OUT OF 16 DECODER USING 3INPUT GATES

FIG. 3.5



1 OUT OF 16 DECODER USING 4 INPUT GATES

FIG 3.6

(iii) a high value of current in a capacitive line. (iv) The transistor should preferally be a NPN transistor. A PNP transistor tends to increase the voltage level by an amount equal to V_{BE}, and the fact that the level shifter is more sensitive to a change in zero level voltage than a change in one level voltage, suggests us not to increase the incoming voltage level.

Transistor SL 100 meets all the above requirements and it is easily available. It is a power transistor with a dissipation of 500mW and current carrying capacity of 500 ma. Moreover it is a NPN transistor. Circuit digram for the buffer x amplifier is shown in figure 3.7. Resistance R_g is introduced to decrease the power dissipation of the transistor.

Taking the supply voltage as + 12V.

R_c (max.) = (12-2.6-0.3)/128 = 9.1(V)/128(ma) = 70

where 2.6 is the minimum 1 level output voltage. Taking into account the variation in transistor saturation voltage V_{ce} and in R_c, we keep R_c as 62

Dissipation in R_c = 62 * $(0.128)^2$

= 1.0W

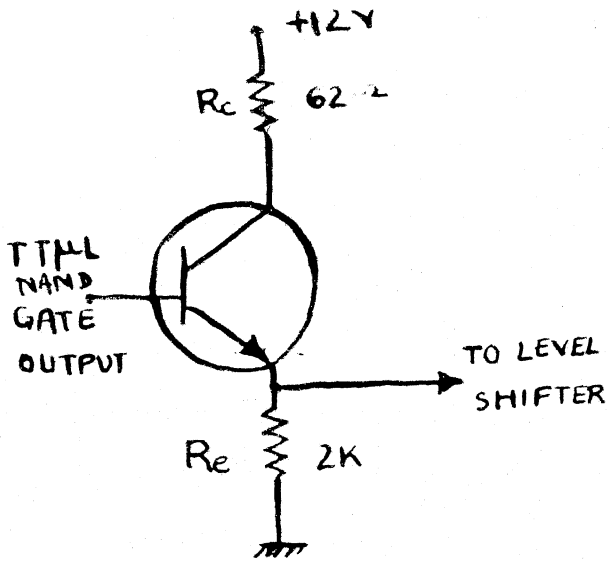
Resistance R_e is a dummy resistor for dc biasing.

(5) Buffer

The incoming information of 16 bits in stored in 16 flip-flops to ensure the availability of channel address through out the process of multiplexing. The storage of information in flip-flops ensures the same treatment for both pulse form and register form of selection input, because we are essentially converting a pulse form input to a level form of selection input.

Another advantage is the availability of information both in true and complement form for all the 16 bits.

By keeping J and K terminals of JK flip-flop at "1" level the



CIRCUIT DIAGRAM OF
BUFFER AMPLIFIER

FIG. 3.7

flip-flop toggles with every positive going input at the clock terminal. This property is made use of for the storage of information.

JK flip-flops have been used as these are easily available in TT L series.

(6) Design of 6 bit Code Circuit

The input to this circuit are the 6 high order bits of incoming information. These bits are compared with the predetermined value of 100000. In case 6 high order bits equal the predetermined value, then a signal known as match signal (Q_c) is generated which enables the rest of the 10 bits to be taken in for decoding purposes.

Thus we have to generate a function Q_c which is $A\,\overline{B\,C\,D\,E\,F}$ where A, B, C, D, E, F are 6 high order bits, starting from the highest order bit.

$$A\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F} = A\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F} * + 0$$

$$= A\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F} + 0$$

$$= A\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F} \,.1$$

$$= (A\,\overline{B}\,\overline{C}) \,.(\overline{D}\,\overline{E}\,\overline{F}) \,.1$$

$$= \left(\overline{\overline{A\,\overline{B}\,\overline{C}} + 0}\right) . (\overline{D}\,\overline{E}\,\overline{F} + 0 \,.\, 1$$

$$= (A\,\bar{B}\,\bar{C}\,.1)\,.\,(\bar{D}\,\bar{E}\,\bar{F}\,.1)\,.1$$

The realisation for Q_c is shown in figure 3.9

(7) Design of Reset Circuit

Any output from digital output terminals of IBM 1800 is brought into the buffer and remains there till a reset pulse is given.

There can be a situation when we are getting some digital output which does not represent the address of a channel. In that case the buffer should be cleared in order to store the next output from IBM 1800 in its true form. So a reset pulse should be generated whenever the device code is not received but some digital output is received at multiplexer input terminals. That is to say if any one or more than one bit is "1" in the digital output and device code is not present, a reset pulse should be generated. Also when the process of multiplexing of a channel is over a reset pulse should reset the system.

Let A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P bet the 16 variables representing the 16 bits input.

Let R be the variable representing the reset pulse. If R is 1 reset pulse is generated.

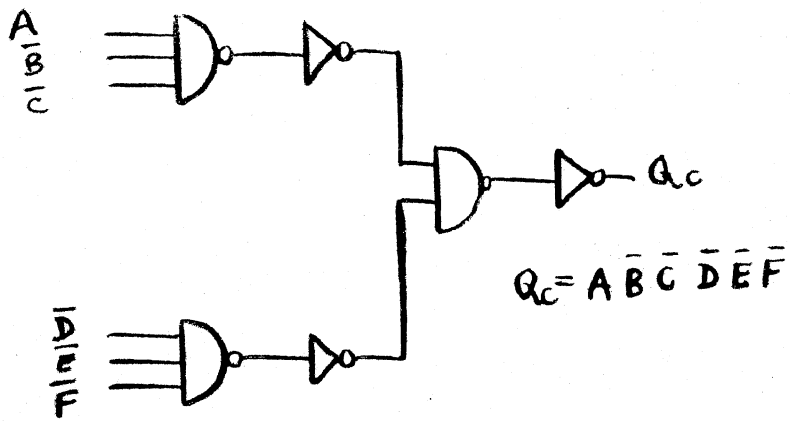
Let $X = A+B+C+D+E+F+G+H+I+J+K+L+M+N+O+P$

and $Q_c = A\,\bar{B}\,\bar{C}\,\bar{D}\,\bar{E}\,\bar{F}$

Putting the two conditions in terms of variables defined above, we get

$$R = X\,\bar{Q}_c\,u(t) + Q_c\,u\,(t-t_1)$$

where t_1 is the time for the process of multiplexing a channel.



REALISATION OF MATCH PULSE (Q_C)

FIG 3·9

Let $X = T0 + T1 + T2 + T3$

where $T0 = A+B+C+D+E+F$

$T1 = G+H$

$T2 = I+J+K+L$

$T3 = M+N+O+P$

Realisation of T0 (see figure 3.10)

$$T0 = A+B+C+D+E+F$$

$$= \overline{\overline{A}\ \overline{B}\ \overline{C}\ \overline{D}\ \overline{E}\ \overline{F}}$$

$$= \overline{(\overline{A}\ \overline{B}\ \overline{C} + 0) \cdot (\overline{D}\ \overline{E}\ \overline{F} + 0)}$$

$$= \overline{\overline{(\overline{A}\ \overline{B}\ \overline{C} + 0)} \cdot \overline{(\overline{D}\ \overline{E}\ \overline{F} + 0)}}$$

$$= \overline{(\overline{A}\ \overline{B}\ \overline{C} \cdot 1) \cdot (\overline{D}\ \overline{E}\ \overline{F} \cdot 1)}$$

Realisation of T1 (see figure 3.11)

$$T1 = G+H = \overline{\overline{G} \cdot \overline{H}}$$

Realisation of T2 (see figure 3.12)

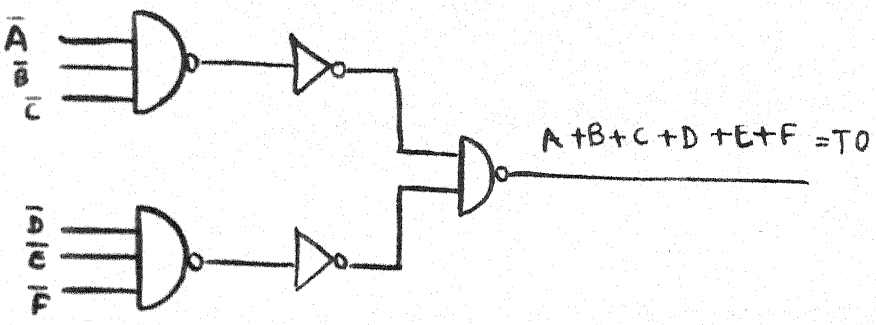
$$T2 = I+J+K+L = \overline{\overline{I}\ \overline{J}\ \overline{K}\ \overline{L}}$$

Realisation of T3 (see figure 3.13)

$$T3 = M+N+O+P = \overline{\overline{M}\ \overline{N}\ \overline{O}\ \overline{P}}$$

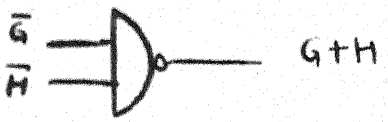
Realisation for X (see figure 3.14)

$$X = \underline{T0} + T1 + T2 + T3$$



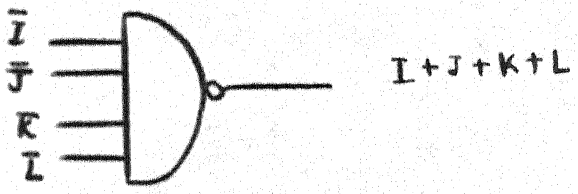
REALIZATION OF TO = A+ B+C +D+E +F

FIG 3·10



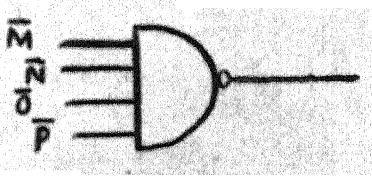
REALIZATION OF T1 = G+H

FIG 3·11



REALIZATION OF T2 = I+J+K+L

FIG 3·12



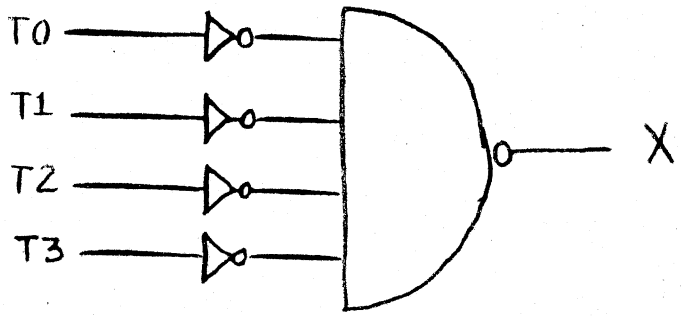
REALIZATION OF T3 = M+N+O+P

FIG 3·13

$$= \overline{\bar{T}0 + \bar{T}1 + \bar{T}2 + \bar{T}3}$$

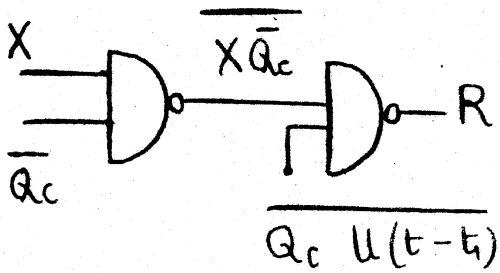
For realisation of R see figure 3.15

By differentiating $\bar{Q}_6$, a monostable is triggered, the output of which is fed into clock terminal of JK flip-flop. The particular type of flip-flop used triggers with positive going clock pulse, so after a time delay of t_1 units the flip-flop output changes to $\overline{Q_6 \cdot u(t - t_1)}$ (see figure 3.16)



REALISATION OF $X = A+B+C+D+E+F+G+H+I+J+K+L+M+N+O+P$

FIG 3.14



GENERATION OF RESET PULSE

FIG 3.15

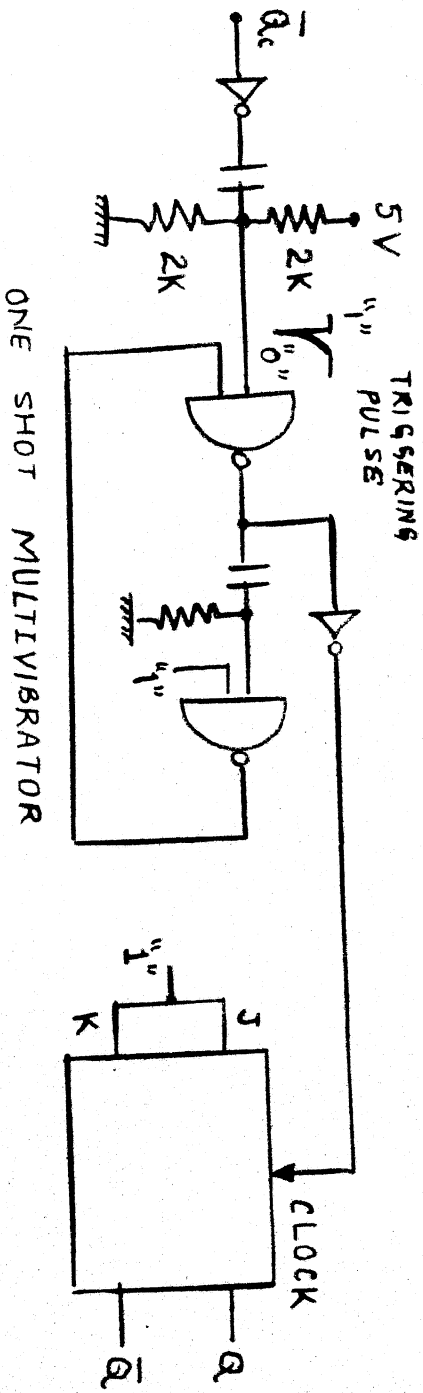

$\bar{Q}_c$
5 V
2K
2K
"1"
"0"
TRIGGERING PULSE
"1"
"1"
ONE SHOT MULTIVIBRATOR
K
J
CLOCK
$\bar{Q}$
Q

FIG 3.16

EXPERIMENTAL RESULTS

1) Performance of Switch

With the analog input of ± 5V dc value, no output voltage was sensed at the output terminals of analog switch. Testing of analog switch without the driving circuitry shows that at a frequency of 200 Kc/s and sinusoidal input of 5V peak voltage a signal of 1 mV of the input frequency appears at the output terminals of field effect transistor. The output voltage of 1 mV decreases as the input frequency decreases, the capacitances between source and gate and gate and drain terminals.

When the analog switch is closed output voltage is same as the input voltage.

Measured rise time of the output signal is 0.8 sec. where as the decay time is 3.2 sec.

2) Sampling Rate

The time for which interface connects the process to the processor depends upon the pulse width of monostable multivibrator. The measured value of pulse width of monostable multivibrator is 12 sec. Accounting for 3 sec. of delay in switching the transistors on, the analog switch remains closed for 9 sec. External synchronisation of this time is not possible.

With 12 sec. as time of closure of analog switch and 3 sec. as the delay caused by driving circuitry, the selection input must stay for a time of 15 sec., which means the maximum sampling rate can be

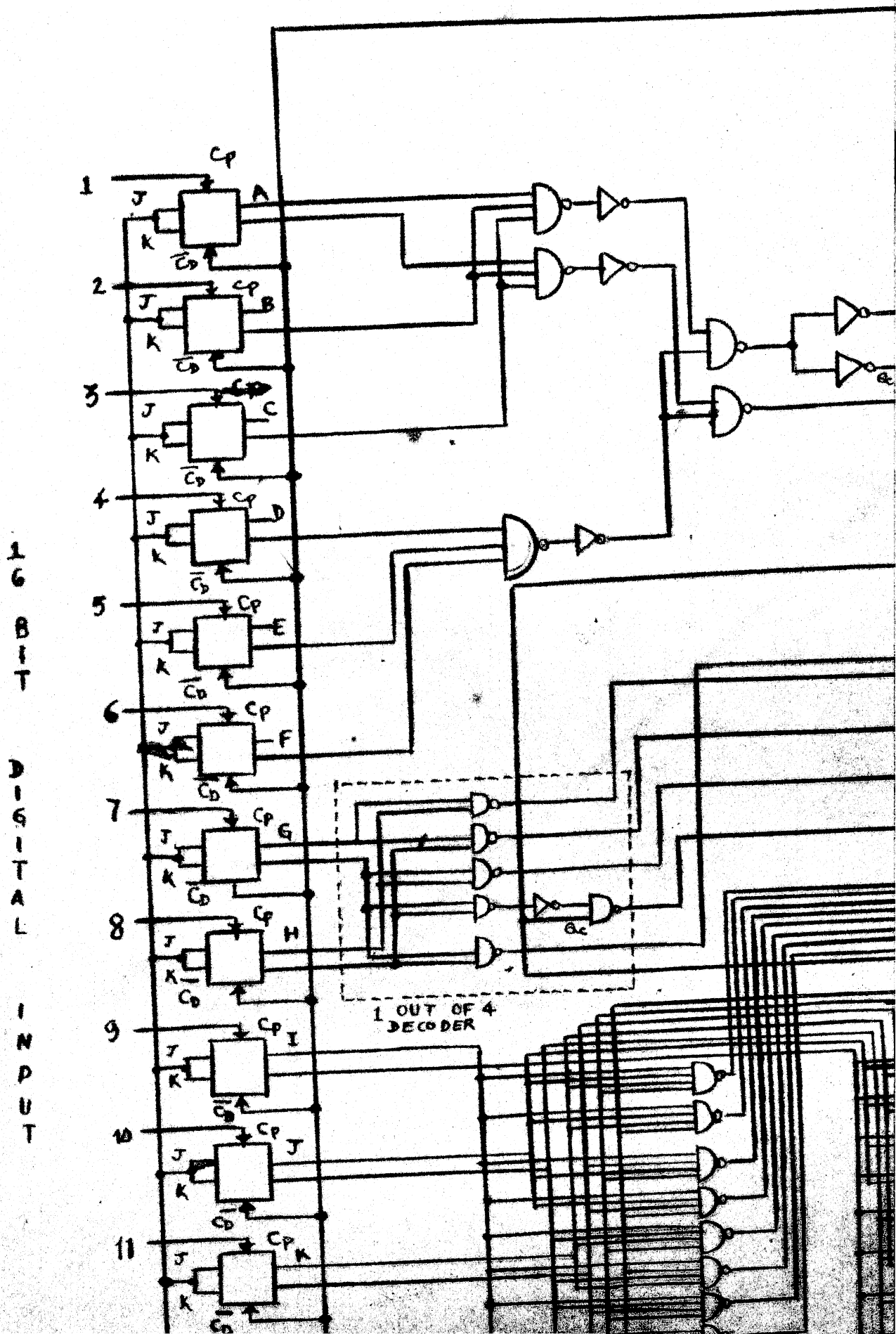
1/15 = 66 K Therefore when sampling rate is less than 66 K only one man line is selected at a time.

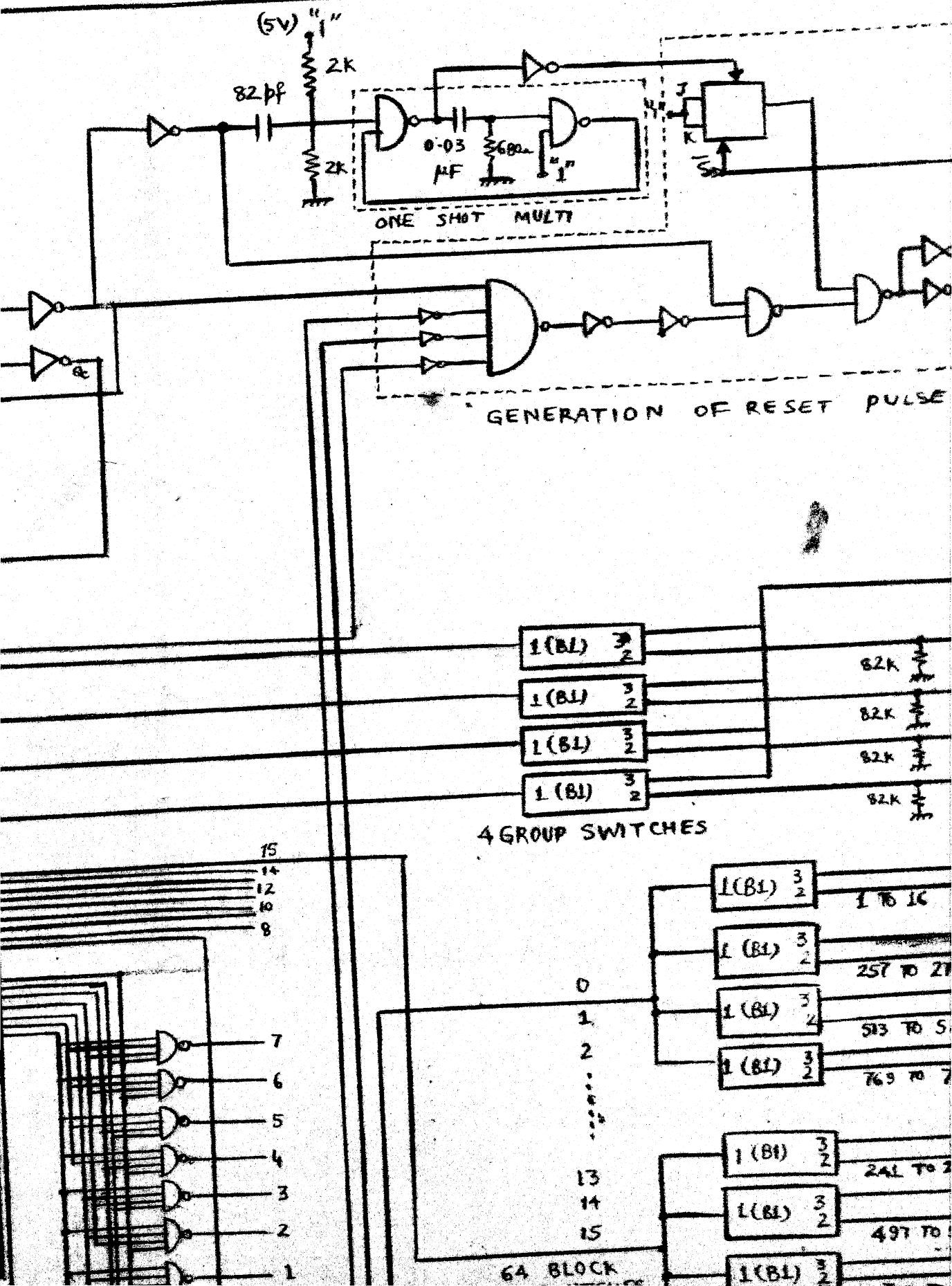
3) Decoding Time

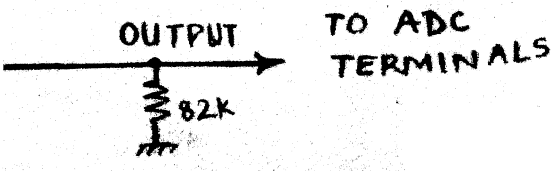
The decoding time of channel address is very small and it is of the order of 40 nsec.

Analog input to the multiplexer should be a single ended input with peak value of signal as 5V

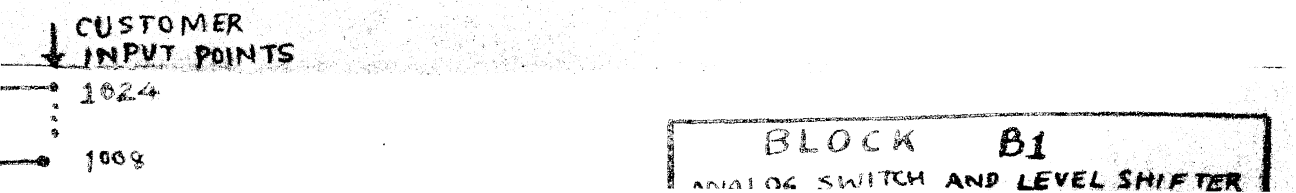
For each thermocouple point a buffer amplifier, which will be an operational amplifier, should be used for connecting it to the analog input point of this multiplexer.


16 BIT DIGITAL INPUT
1
2
3
4
5
6
7
8
9
10
11
J
K
Cp
$\overline{C_D}$
A
B
C
D
E
F
G
H
I
J
K
1 OUT OF 4 DECODER


(5V) "1"
2K
82 pf
2K
0·03 μF
680Ω
"1"
ONE SHOT MULTI
J
K
GENERATION OF RESET PULSE
1 (BL) 3/2
1 (BL) 3/2
1 (BL) 3/2
1 (BL) 3/2
82K
82K
82K
82K
4 GROUP SWITCHES
15
14
12
10
8
7
6
5
4
3
2
1
0
1
2
13
14
15
64 BLOCK
1 (BL) 3/2
1 (BL) 3/2
1 (BL) 3/2
1 (BL) 3/2
1 TO 1C
257 TO 2
513 TO 5
769 TO 7
1 (BL) 3/2
1 (BL) 3/2
1 (BL) 3/2
241 TO
497 TO



JK FLIP FLOP (DUAL)	9024
4 INPUT NAND GATE (DUAL)	7420
3 INPUT NAND GATE (TRIPLE)	7410
2 INPUT NAND GATE (QUAD)	7400
INVERTERS	9016



4 INPUT NAND GATE (DUAL)	7420
3 INPUT NAND GATE (TRIPLE)	7410
2 INPUT NAND GATE (QUAD)	7400
INVERTERS	9016

STOMER
PUT POINTS
024
08

CUSTOMER INPUT POINTS (ANALOG VOLTAGE INPUT)

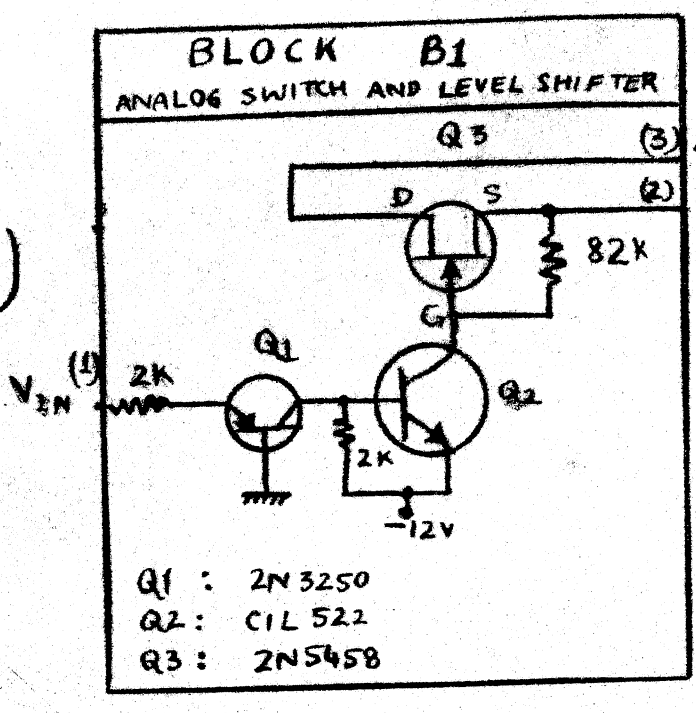
2

5

1009

993

17



CONCLUSIONS

The main feature of this solid state multiplexer is the use of field effect transistors, which

(i) minimizes the offset voltage

(ii) increases the frequency response of the system

(iii) increases the sampling rate of the multiplexer.

By keeping gate-to-source voltage as zero, offset voltage even in microvolt is not there.

Without the use of sample and hold amplifier or any other amplifier at the output terminals of multiplexer, high sampling rates can be achieved. For example, with a sample time of 12 microseconds sampling rate can be as high as 50 K c/s which is a very high speed. Against this we find in IBM 1800 computer the 1826 multiplexer unit with 'SAMPLE AND HOLD AMPLIFIER' giving sampling rates of 20 K c/s. The limit of 20 K c/s/ in the 1826 multiliexer unit is because of transistors used in the circuit. Whereas in the other multiplexer speed is limited not become of FET switches but because of ADC.

Another feature of this multiplexer is asynchronous input, automatic resetting and high speed of decoding of channel address. These facilities are provided by using the digital integrated circuits. Transistor transistor micro logic digital integrated circuits reduce the decoding time to a value less than 40 nanoseconds. The system resets itself for the next input in less than 100 nsec.

Following are the drawbacks in this multiplexer unit.

(i) Since the monostable multivibrator is constructed using digital integrated circuits, so the pulse width varries with the supply voltage. But this variation in pulse width can be reduced by using a very stable and regulated power supply.

(ii) The field effect transistor switches are off when negative supply of - 12 V is applied at their gate terminals. But if somehow this negative voltage is removed from FET gate, the switch is closed. Thus if the power supply to the multiplexer unit fails, all the FET switches are closed, which in turn short circuits the output of all transducers. This problem has been solved at the cost of accuracy by putting a series resistance of 2 K in series with each channel. This circuited to each other.

Overall this multiplexer unit is very cheap as compared to other solid state multiplexer employing bipolar transistors and pulse transformers as analog switch. Also there is no need of sample and hold amplifier for feeding in ADC.

GENERAL REFERENCES

1. David F. Hoeschele Jr. : Analog to digital and Digital to Analog Conversion Techniques. Chap 3 (Book) McGrawHill

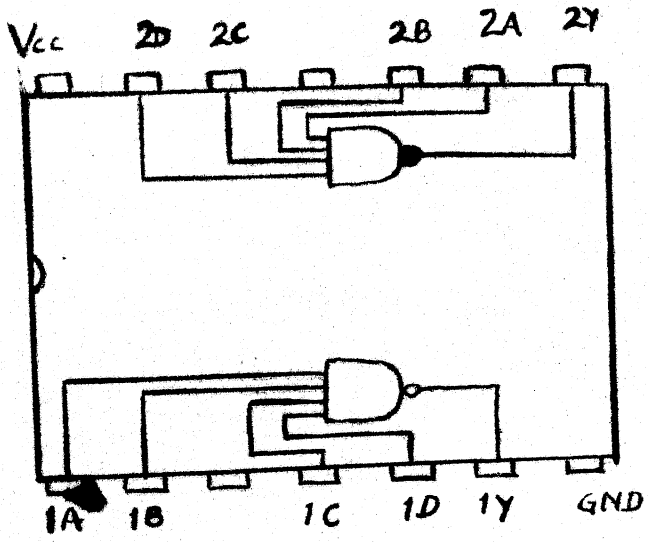
2. IBM 1800 Manual : Physical Order Planning Order No. GA26 5922

APPENDIX A

	Collector Base Voltage BV_{CBO}	Collector Emitter Voltage BV_{CEO}	Emitter Base Voltage V_{EBO}	Average Collector Current (mA)	Dissipation 25 C Ambient Temperature	V_{CE}(sat.)	V_{BE}(sat.)
2N 3250	50 V I_C = 10 A	40 V	5 V I_E = 10 A	200	0.36 W	0.25 V I_C = 10mA I_B = 1mA	0.9 V I_C = 10mA I_B = 1mA
CIL522	32 V	32 V	5 V	100	0.5W		
SL 100	60 V	50 V	7 V		2.8 W	0.6 V I_C = 150mA I_B = 15mA	

APPENDIX B

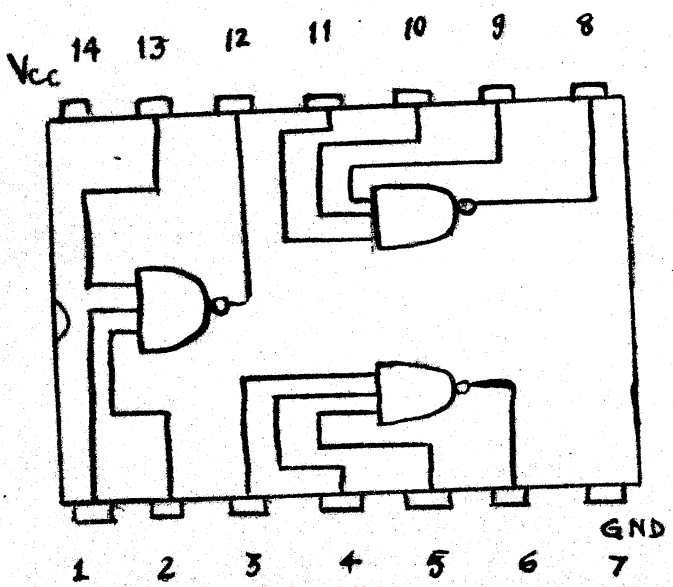
BASE CONNECTIONS OF DIGIT CIRCUITS



POSITIVE LOGIC

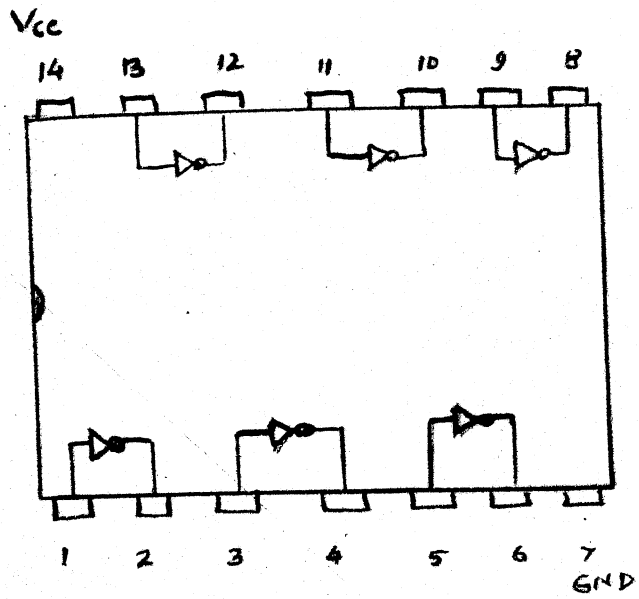
$$Y = \overline{ABCD}$$

SN 7420

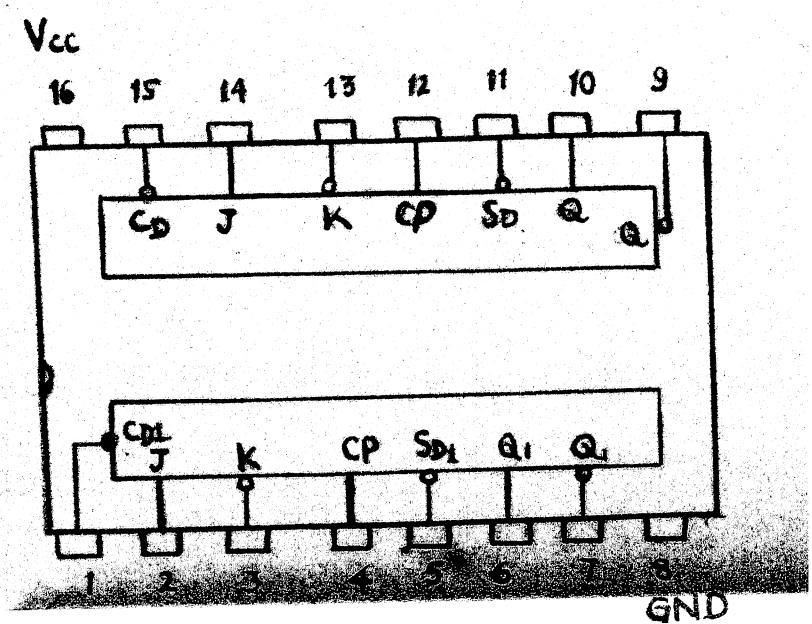


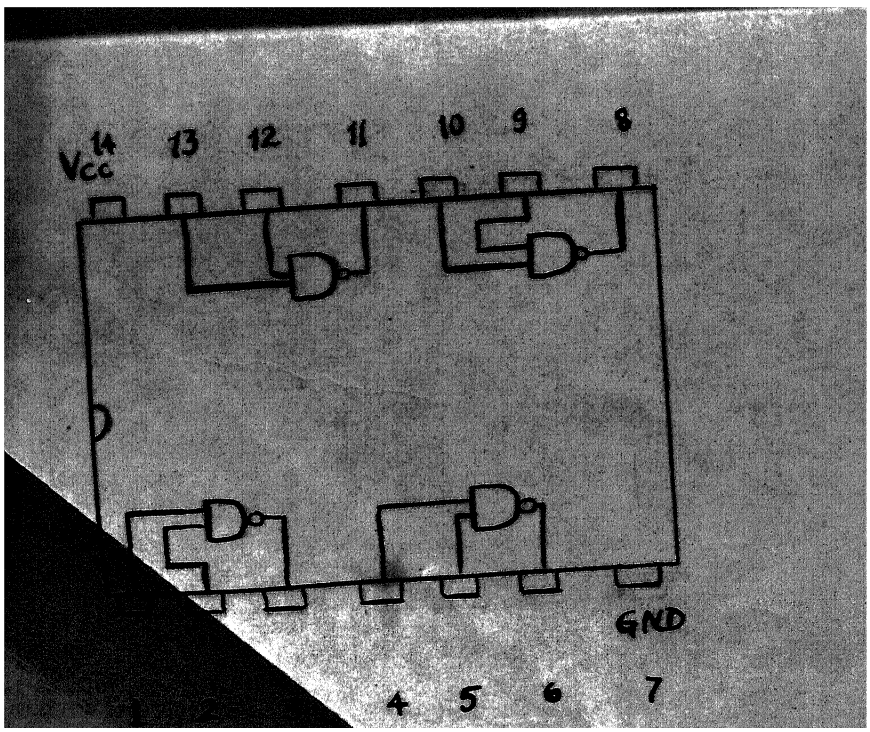
SN 7410

OF DIGITAL INTEGRATED



9016




14
Vcc
13
12
11
10
9
8
GND
4
5
6
7

Date Slip

This book is to be returned on the date last stamped.

CD 6.72.9

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EE-1972-~~D~~M-MAN-MUL